An MMIC Low-Distortion Variable-Gain Amplifier Using Active Feedback

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Abstract

A new low-distortion variable-gain amplifier (VGA) is proposed and analyzed. The gain of the VGA is controlled using the transconductance of a common-drain FET (CDF) in the negative feedback path. The analysis and prototype results indicate that the third-order intermodulation-distortion ratio is greatly improved at a high input power levels due to the CDF's unilateral characteristic and a reduction in the VGA's input impedance.

I. Introduction

Variable-gain amplifiers (VGAs) are used in radio communication equipment to control the input power level of mixers because the power level of the received signals varies widely. The dynamic range of a receiver is limited at the low signal-level end by its noise figure performance and at the high signal-level end by its linearity. Recently, the maximum received-signal-level requirement has increased, and is approaching -5 to 0 dBm. This means VGAs must have a wider gain-control range and greater linearity.

Conventional VGAs utilize the gate-bias or drain-bias dependence of FET transconductance (g_m) [1],[2]. Their disadvantage is that they exhibits poor linearity under compressed gain conditions. This is because FET linearity degrades as g_m decreases. Another recently reported VGA is a variable-resistance negative-feedback amplifier using an FET varistor [3],[4]. The linearity of this amplifier is better than that of conventional amplifiers. This is because the varistor's impedance is decreased as the input power level increases in order to suppress the applied voltage for amplification at the FET's gate terminal. However, the minimum variable resistance is limited by the FET-varistor gate-width, to about 40 Ω for a 100-μm gate FET [3],[4], and expansion of the FET gate-width degrades the VGA performance due to the increase in parasitic capacitance. Furthermore, the FET varistor is not unilateral conductivity. For these reasons, the maximum received-signal level remains limited to -10 dBm.

To overcome the above mentioned problems, the authors proposed a new negative feedback variable-gain amplifier that utilizes a common-drain FET (CDF) in the feedback path [5]. The gain of the new VGA is controlled by CDF transconductance. This paper presents a detailed analysis of the gain and distortion of the new VGA. In addition measured performance of a fabricated VGA is shown.

II. Basic theory

A. Gain characteristic

The basic configuration of the new VGA is shown in Fig. 1 (a). The VGA consists of a FET for amplification, a common-drain FET for feedback path control, capacitors, and matching circuits. Features of the common-drain FET are a high constant-gate impedance, a widely-variable source-impedance ($1/g_m$), and a unilateral characteristic (from gate to source). Figure 1 (b) shows a simplified equivalent circuit for the amplification and the feedback path. The Y matrixes of the amplifying FET (common-source FET) and the common-drain FET in the feedback path are

$$[Y_{CSF}] = \begin{bmatrix} j\omega C_{gs} & 0 \\ G_{m0} & G_d \end{bmatrix} \quad (1)$$

$$[Y_{CDF}] = \begin{bmatrix} g_m & -g_m \\ 0 & 0 \end{bmatrix} \quad (2)$$

respectively. The Y matrix of the equivalent circuit is

$$[Y] = \begin{bmatrix} j\omega C_{gs} + g_m & -g_m \\ G_{m0} & G_d \end{bmatrix} \quad (3)$$

where, g_m is the transconductance of the common-drain FET in the feedback path, G_{m0}, C_{gs}, and G_d are the transconductance, the gate-source capacitance and the drain conductance of the amplifying FET, respectively. The Y matrix (2) shows the unilateral transmission in the common-drain FET. From the Y matrix (3) amplifier gain S_{21} and input impedance Z_{in} are obtained as following:

$$S_{21} = \frac{-2 G_{m0} Z_0}{1 + Z_0 G_d + \left(1 + Z_0 G_d + Z_0 G_{m0}\right) Z_0 g_m + j\omega Z_0 C_{gs} \left(1 + Z_0 G_d\right)} \quad (4)$$

$$\approx \frac{-2 G_{m0} Z_0}{1 + \left(1 + Z_0 G_{m0}\right) Z_0 g_m}$$

and

$$Z_{in} = \frac{1 + Z_0 G_d}{\left(1 + Z_0 G_d + Z_0 G_{m0}\right) g_m + j\omega C_{gs} \left(1 + Z_0 G_d\right)} \quad (5)$$

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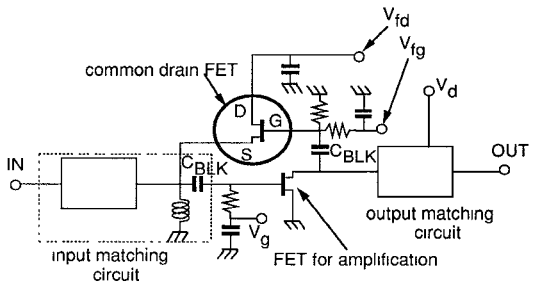
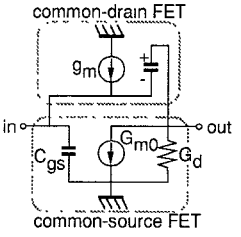


(a)



(b)

Fig. 1 Basic configuration.
(a) Basic configuration of the common-drain FET feedback VGA.
(b) Equivalent circuit for the amplification and the feedback path.

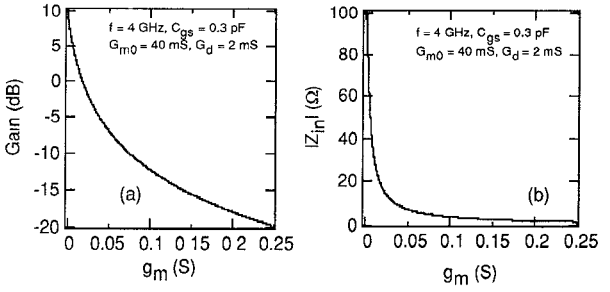


Fig. 2 CDF feedback VGA performance
(a) Gain characteristic. (b) Input impedance characteristic.

$$\approx \frac{1}{(1+Z_0\,G_{m0})\,g_m}$$

The above expressions show that the gain and the input impedance of the VGA can be changed by controlling the transconductance of the CDF in the feedback path. When the CDF is biased at the pinch-off voltage, $g_m = 0$, VGA gain S_{21} is maximized. Figure 2 shows the gain and the input impedance characteristics of the CDF feedback VGA. Both the gain and the input impedance decrease as CDF transconductance, g_m, increases. The dependence of the gain and input impedance on the transconductance is similar to their dependence on the variable resistance in the varistor feedback VGA.

B. Distortion characteristic

The simple circuit model used to analyze the distortion characteristic is shown in Fig. 3 with load admittance G_L, the source impedance Z_0, the transconductance of the CDF g_m, the transconductance of the amplifying FET G_m and the drain

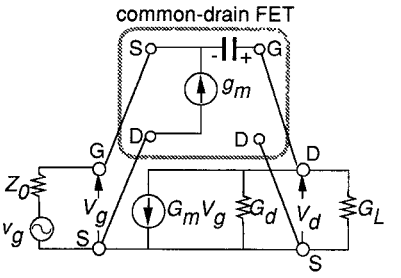


Fig. 3 Simplified equivalent circuit model for distortion analysis

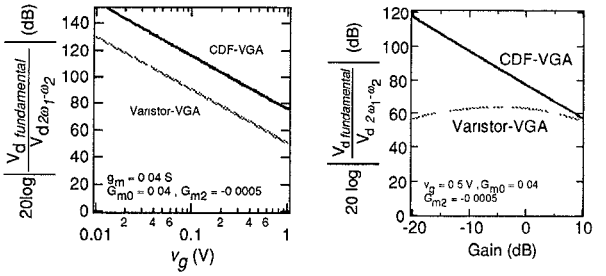


Fig. 4 D/U performances of the CDF feedback VGA.
(a) D/U versus input power voltage. (b) D/U versus VGA gain

conductance of the amplifying FET G_d. Voltages v_g, V_g and V_d are the input voltage, the gate voltage and the drain voltage, respectively.

The analysis used here is based on a power-series description [6],[7] of only the transconductance nonlinearity of the amplifying FET. The transconductance nonlinearity is principally determined by the gate voltage. The voltage dependence of this characteristic may be represented by a power series of the form

$$G_m = G_{m0} + G_{m1} V_g + G_{m2} V_g^2. \tag{6}$$

Intermodulation is defined for the case of two equal amplitude sinusoidal signals at frequencies ω_1 and ω_2. Considering the input impedance, Z_{in}, of the CDF feedback VGA, the gate bias V_g is

$$V_g = A\,v_g\left(\cos(\omega_1 t) + \cos(\omega_2 t)\right) \tag{7}$$

where

$$A = \frac{Z_{in}}{Z_{in}+Z_0}. \tag{8}$$

The third-order intermodulation products are generated at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$.

The first-order output at the fundamental frequency ω_1 is

$$V_{d\,fundamental} = -\frac{1}{G_L+G_d}\left[G_{m0}\,A\,v_g + \frac{9}{4}\,G_{m2}\,(A\,v_g)^3\right]\cos(\omega_1 t) \tag{9}$$

and the third-order intermodulation output at frequency $2\omega_1 - \omega_2$ is

$$V_{d\,2\omega_1-2\omega_2} = -\frac{1}{G_L+G_d}\,\frac{3}{4}\,G_{m2}\,(A\,v_g)^3\cos\left((2\omega_1-\omega_2)t\right). \tag{10}$$

The third-order intermodulation distortion ratio, D/U, is defined as the ratio of the distortion output power at $2\omega_1 - \omega_2$ to that at fundamental frequency ω_1. The D/U may be expressed using expressions (9) and (10) as:

$$D/U = 20\log\left|\frac{V_{d\,fundamental}}{V_{d\,2\omega_1-\omega_2}}\right|$$

$$= 20\log\left|\frac{G_{m0}Av_g + \frac{9}{4}G_{m2}(Av_g)^3}{\frac{3}{4}G_{m2}(Av_g)^3}\right|. \qquad (11)$$

The D/U of the varistor feedback VGA is obtained by utilizing the same analysis and replacing the part of the common-drain FET in Fig. 3 with the variable resistor. The D/U of the varistor feedback VGA is expressed by changing $G_{m0}Av_g$ to $(G_{m0} - 1/R_{fb})Bv_g$, where R_{fb} is the variable resistance.

$$D/U = 20\log\left|\frac{\left(G_{m0} - \frac{1}{R_{fb}}\right)Bv_g + \frac{9}{4}G_{m2}(Bv_g)^3}{\frac{3}{4}G_{m2}(Bv_g)^3}\right| \qquad (12)$$

The gain of the varistor feedback VGA decreases as R_{fb} decreases. Expression (12) has a parameter to decrease the D/U of VGA, $G_{m0} - 1/R_{fb}$, while Expression (11) has a constant parameter, G_{m0}. Therefore, D/U of the CDF feedback VGA is higher than that of the varistor feedback VGA. This is because the feedback path constructed by the CDF has the unilateral characteristic. In addition, the difference in D/U between the CDF feedback VGA and the varistor feedback VGA increases under the compressed gain condition.

Figure 4 (a) compares the dependence of D/U on the input power, v_g, for the CDF feedback VGA and the varistor feedback VGA. These results were calculated by utilizing the above expressions. Figure 4 (b) compares the D/U versus the gain of VGAs at the input power of v_g = 0.5 V. The D/U of the CDF feedback VGA is higher than that of the varistor feedback VGA. These results show that the linearity of the CDF feedback VGA is better than that of the varistor feedback VGA.

III. Fabrication

A micro-photograph of a 4-GHz CDF feedback VGA is shown in Fig. 5. The VGA uses cascode-connected FETs with 200-μm gate width for amplification and a 200-μm gate FET for the CDF in the feedback path. The chip size is 1.41 mm x 1.43 mm. V_{fg} and V_{fd} are the controlled biases for the common-drain FET, and V_d, V_g, and V_c are the drain bias, the gate bias (which is constant at 0 V), and the second gate bias for the cascode-connected FETs, respectively.

Figure 6 shows the measured variable-gain performance of the VGA. The gain varies more than 15 dB in the 3 to 4.5-GHz frequency range, for gain-control-voltages, V_{fg}, from -7 to 0 V. A three stage VGA provides a sufficient gain-control range for digital radio systems[4]. Figure 7 (a) and (b) shows the input return losses (S_{11}) and the output return losses (S_{22}) in the control voltage range. The variation of $|S_{22}|$ is less than 3.5 dB peak-to-peak over the frequency range. The input return loss, $|S_{11}|$,

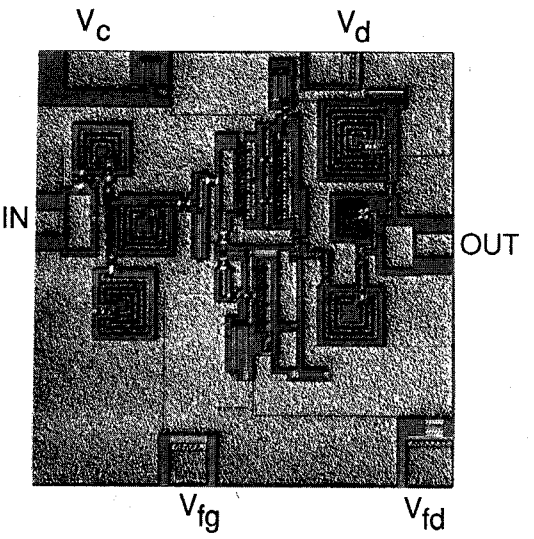


Fig. 5 Micro-photograph of the 4-GHz CDF feedback VGA. Chip size is 1.41 mm x 1.43 mm.

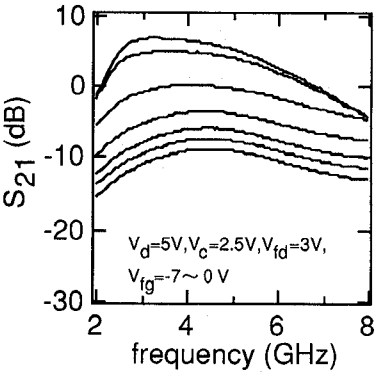


Fig. 6 Variable gain performance.

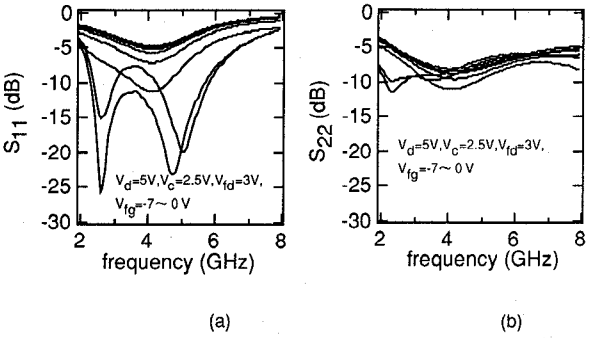


Fig. 7 Return loss performance.
(a) Input return losses.
(b) Output return losses.

decreases as the control voltage varies from -7 to 0 V because the input impedance of the CDF feedback VGA decreases.

Figure 8 compares the D/U versus input power characteristics at the minimum gain, for the CDF feedback VGA and the varistor feedback VGA. The varistor feedback VGA is designed to have similar gain-frequency characteristics and the same minimum input impedance as the CDF feedback VGA. The D/U of the CDF feedback VGA is 15 dB higher than that of the varistor feedback VGA. The input power improvement is more than 8 dB at a D/U of 50 dB. This indicates that the CDF feedback VGA provides linear variable-gain amplification to an input power level of 0 dBm.

Figure 9 shows the linearity of the CDF feedback VGA at various control voltages. Black circles indicate the maximum input power satisfying the D/U of 50 dB and white circles show corresponding amplifier gain. The region under the D/U curve indicates linear operation (D/U > 50 dB). The maximum input power increases at V_{fg} from -5.8 V to 0 V although it degrades at V_{fg} from -8 V to -5.8 V. The maximum input power at the minimum gain is distinctly higher than that at the maximum gain. Such significant improvement is not possible with conventional VGAs.

Above measured results exhibit that the CDF feedback VGA has higher linearity and that the analysis is correct.

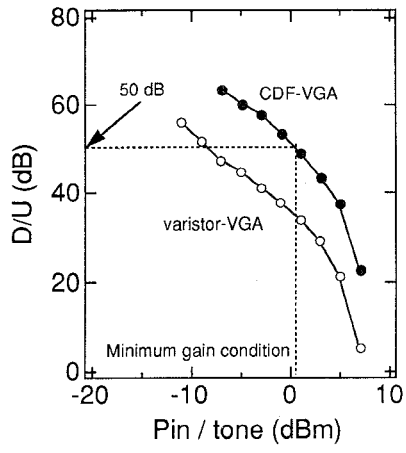


Fig. 8 Measured D/U versus input power level.

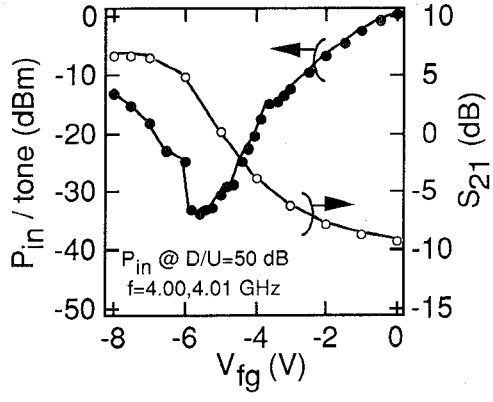


Fig. 9 Maximum input power and associated gain of the CDF feedback VGA over control voltages between -8 V and 0 V.

IV. Conclusion

The common-drain FET feedback variable-gain amplifier was proposed and demonstrated. VGA gain is controlled using the transconductance of the CDF placed in the feedback path. An analysis indicates that the third-order intermodulation distortion ratio of the CDF feedback VGA is drastically improved due to the unilateral conductivity of the CDF. The measured data confirm that the CDF feedback VGA has higher linearity under compressed gain conditions than conventional VGAs.

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